AMENDMENTS TO THE CLAIMS

1. (Currently amended) A pixel sensor cell comprising:

a substrate;

a photoconversion device comprising a region of a first conductivity type at a surface of the substrate and a region of a second conductivity type below the first conductivity type region, said photoconversion device having a pinning voltage;

a gate, wherein at least a portion of said gate is located directly over said photoconversion device for changing said pinning voltage;

a charge collection region for receiving charges from said photoconversion device; and

a transistor for transferring charge from said photoconversion device to said charge collection region.

2. (Previously presented) A pixel sensor cell comprising:

a substrate;

a photoconversion device comprising a region of a first conductivity type at a surface of the substrate and a region of a second conductivity type below the first conductivity type region;

a gate located over said photoconversion device;

a charge collection region for receiving charges from said photoconversion device; and

a transistor for transferring charge from said photoconversion device to said charge collection region,

wherein said pixel sensor cell is arranged such that said photoconversion device has a reduced pinning voltage (V_{PIN}) when a negative bias is applied to said gate.

3. (Original) The pixel sensor cell according to claim 2 wherein said gate reduces an energy barrier between said photoconversion device and said charge collection region.

4. (Currently amended) The pixel sensor cell according to claim 1 wherein said gate comprises a dielectric ~~substance~~ layer and a polysilicon layer.

5. (Canceled).

6. (Previously presented) The pixel sensor cell according to claim 1 wherein said photoconversion device comprises a pinned photodiode.

7. (Previously presented) The pixel sensor cell according to claim 1 wherein said charge collection region comprises a floating diffusion region.

8. (Previously presented) A pixel sensor cell comprising:

a substrate having a first surface level;

a photoconversion device having a first doped region of a first conductivity type and a second doped region of a second conductivity type located within said substrate, said photoconversion device having a pinning voltage;

a dielectric substance layer formed over the first surface level of said substrate thereby forming a second surface level;

a polysilicon layer formed over said second surface level;

a contact connected to said polysilicon layer for using a voltage to change said pinning voltage; and

a transistor located adjacent to said photoconversion device.

9. (Original) The pixel sensor cell according to claim 8 wherein said dielectric substance layer has a thickness in the range of about 50-150 Å.

10. (Previously presented) The pixel sensor cell according to claim 8 wherein said dielectric substance layer comprises silicon dioxide.

11. (Previously presented) The pixel sensor cell according to claim 8 wherein said dielectric substance layer comprises silicon nitride (Si_3N_4).

12. (Previously presented) The pixel sensor cell according to claim 8 wherein said dielectric substance layer comprises silicon oxynitride (SiON).

13. (Original) The pixel sensor cell according to claim 8 wherein said polysilicon layer has a thickness in the range of about 500-1500 Å.

14. (Previously presented) The pixel sensor cell according to claim 8 wherein said polysilicon layer comprises silicon germanium.

15. (Previously presented) The pixel sensor cell according to claim 14 wherein said polysilicon layer comprises silicon germanium in a ratio of about $Si_{60}Ge_{40}$.

16. (Previously presented) The pixel sensor cell according to claim 8 wherein said transistor comprises a transfer transistor.

17. (Original) The pixel sensor cell according to claim 8 wherein said polysilicon layer overlaps at least a portion of said transistor.

18. (Original) The pixel sensor cell according to claim 8 wherein said pixel sensor cell is part of a CMOS imager.

19. (Original) The pixel sensor cell according to claim 8 wherein said pixel sensor cell is part of a charge coupled device (CCD) imager.

20. (Previously presented) An imager comprising:

an array of pixel sensor cells, each pixel sensor cell having a photodiode device;

a substrate having a first surface level, said photodiode devices being located within said substrate and comprising a region of a first conductivity type at a surface of the substrate and a region of a second conductivity type below the first conductivity type region;

photodiode gates located over said substrate first surface level and over respective said photodiode devices; and

signal processing circuitry formed in said substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing said image,

wherein each said pixel sensor cell is arranged such that a photodiode therein has a reduced pinning voltage (V_{PIN}) when a negative bias is applied to an associated photodiode gate.

21. (Original) The imager according to claim 20 wherein said photodiode gate further comprises a dielectric substance layer and a polysilicon layer.

22. (Original) The imager according to claim 20 wherein said imager is a CMOS imager.

23. (Original) The imager according to claim 20 wherein said imager is a charge coupled device (CCD) imager.

24. (Currently amended) A processing system comprising:

a processor; and

an imager coupled to said processor, said imager comprising an array of pixel sensor cells, each pixel sensor cell comprising:

a photoconversion device located within a substrate and comprising a region of a first conductivity type at a surface of the substrate and a region of a second conductivity type below the first conductivity type region and said photoconversion device having a pinning voltage[[,]] ;

a gate located over said substrate ~~first surface level~~ and at least a portion of said gate being located directly over said photoconversion device for changing said pinning voltage; and

a readout circuit for said photoconversion device comprising at least an output transistor.

25. (Previously presented) The system according to claim 24 wherein said gate further comprises a dielectric layer and a polysilicon layer.

26. (Original) The system according to claim 24 wherein said imager is a CMOS imager.

27. (Original) The system according to claim 24 wherein said imager is a charge coupled device (CCD) imager.

28. (Previously presented) A method of forming a sensor, comprising:

forming a substrate having a first surface level;

forming a photoconversion device with a pinning voltage (V_{PIN}), said photoconversion device having a first doped region of a first conductivity type and a second doped region of a second conductivity type beneath said first surface level of said substrate;

forming a gate for changing said pinning voltage comprising a dielectric layer over said first surface level of said substrate, thereby forming a second surface level, and a polysilicon layer over said dielectric layer; and

forming a charge collection region for receiving charges from said photoconversion device.

29. (Canceled).

30. (Previously presented) A method of forming a sensor, comprising:

forming a substrate having a first surface level;

forming a photoconversion device with a pinning voltage (V_{PIN}), said photoconversion device having a first doped region of a first conductivity type and a second doped region of a second conductivity type beneath said first surface level of said substrate;

forming a photodiode gate including a dielectric layer over said first surface level of said substrate, and a polysilicon layer over said dielectric layer;

connecting a contact to said photodiode gate; and

forming a charge collection region for receiving charges from said photoconversion device;

wherein said photodiode gate is operable to reduce an energy barrier between said photoconversion device and said charge collection region.

31. (Currently amended) The method according to claim 28 wherein said dielectric ~~substance~~ layer has a thickness in the range of about 50-150 Å.

32. (Currently amended) The method according to claim 28 wherein said dielectric ~~substance~~ layer comprises silicon dioxide.

33. (Currently amended) The method according to claim 28 wherein said dielectric ~~substance~~ layer comprises silicon nitride (Si_3N_4).

34. (Currently amended) The method according to claim 28 wherein said dielectric ~~substance~~ layer comprises silicon oxynitride (SiON).

35. (Original) The method according to claim 28 wherein said polysilicon layer has a thickness in the range of about 500-1500 Å.

36. (Original) The method according to claim 28 wherein said polysilicon layer is formed of silicon germanium (SiGe).

37. (Original) The method according to claim 36 wherein said silicon germanium has a ratio of about $Si_{60}Ge_{40}$.

38. (Previously presented) The method according to claim 28 wherein said charge collection region comprises a floating diffusion region.

39. (Currently amended) The method according to claim 28 further comprising forming a transfer transistor.

40. (Previously presented) The method according to claim 39 wherein said polysilicon layer overlaps at least a portion of said transistor.

41. (Original) The method according to claim 28 wherein said sensor is part of a CMOS imager.

42. (Original) The method according to claim 28 wherein said sensor is part of a charge coupled device (CCD) imager.

43. (Currently amended) The imager according to claim 20 wherein ~~said pixel sensor cells are arranged such that said photoconversion devices have a reduced pinning voltage (V_{PIN}) when a negative bias is applied to said contacts~~ said negative bias is applied to a contact connected to said photodiode gate.

44. (Currently amended) The imager according to claim 20 wherein said gates reduce an energy barrier between said ~~photoconversion~~ photodiode devices and [[said]] charge collection regions for receiving charges from said photodiode devices.

45. (Currently amended) The system according to claim 24 wherein said pixel sensor cell is arranged such that said photoconversion device has a reduced pinning voltage (V_{PIN}) when a negative bias is applied to said ~~contact~~ gate.

46. (Currently amended) The system according to claim 24 wherein said gate reduces an energy barrier between said photoconversion device and [[said]] a charge collection region for receiving charges from said photoconversion device.

47. (Previously presented) A pixel sensor cell comprising:

a substrate;

a photoconversion device comprising a region of a first conductivity type at a surface of the substrate and a region of a second conductivity type below the first conductivity type region;

a gate located directly over at least a portion of and in a plane vertical to said photoconversion device;

a contact connected to said gate;

a charge collection region for receiving charges from said photoconversion device; and

a transistor for transferring charge from said photoconversion device to said charge collection region,

wherein said pixel sensor cell is arranged such that said photoconversion device has a reduced pinning voltage (V_{PIN}) when a negative bias is applied to said contact.

48. (Previously presented) The pixel sensor cell according to claim 47, wherein said gate is configured to reduce an energy barrier between said photoconversion device and said charge collection region.

49. (Currently amended) A method of operating a sensor pixel, said sensor pixel comprising:

a substrate having a first surface level;

a photoconversion device with a pinning voltage (V_{PIN}), said photoconversion device having a first doped region of a first conductivity type and a second doped

region of a second conductivity type beneath said first surface level of said substrate; and

a gate including a dielectric layer and a conductive layer over said first surface level of said substrate,

wherein a negative bias is applied to said gate, such that said gate acts to reduce said pinning voltage (V_{PIN}) of said photoconversion device.

50. (Canceled).